What is claimed is:

1. A lead frame comprising:

a die pad on which a semiconductor chip having an active surface where a plurality of electrode pads are formed is mounted;

a plurality of inner leads electrically interconnected to corresponding electrode pads by a plurality of bonding wires;

a side ring pad disposed around the die pad and between the die pad and the inner leads; and

a tie bar arranged to connect the die pad and the side ring pad,

wherein said plurality of electrode pads includes power electrode pads which are electrically interconnected to the side ring pad by power bonding wires.

2. The lead frame as claimed in claim 1, wherein the die pad, the inner leads, and the tie bar are made of the same metal.

3. The lead frame as claimed in claim 1, further comprising a plurality of outer leads made in one body with the plurality of inner leads.

4. The lead frame as claimed in claim 1, wherein the tie bar include a bent portion arranges to maintain the co-planarity of the semiconductor chip and the inner leads.

5. The lead frame as claimed in claim 4, wherein the die pad, the inner leads, and the tie bar are made of the same metal.

6. The lead frame as claimed in claim 4, further comprising a plurality of outer leads made in one body with the plurality of inner leads.

7. A lead frame comprising:

a die pad on which a semiconductor chip having an active surface where a plurality of electrode pads are formed is mounted;

a plurality of inner leads electrically interconnected to corresponding electrode pads by a plurality of bonding wires;

a side ring pad disposed around the die pad and between the die pad and the inner leads; and

a tie bar arranged to connect the die pad and the side ring pad,

wherein said side ring pad includes a plurality of conductive pads formed thereon.

8. The lead frame as claimed in claim 7, wherein the plurality of bonding wires include first link bonding wires connected between the electrode pads and the conductive pads and second link boding wires connected between the conductive pads and the inner leads.

9. The lead frame as claimed in claim 8, wherein inner leads to which both the first and the second link bonding wires are bonded are disposed at corners of the lead frame.

10. A semiconductor chip package comprising:

a semiconductor chip having an active surface where a plurality of electrode pads are formed;

a lead frame having a plurality of leads;

a plurality of bonding wires electrically interconnecting the electrode pads and corresponding leads;

an encapsulant covering the semiconductor chip, thereby forming a package body;

said lead frame comprising:

a die pad on which the semiconductor chip is mounted;

a plurality of inner leads electrically interconnected to corresponding electrode pads by a plurality of bonding wires;

a side ring pad disposed around the die pad and between the die pad and the inner leads; and

a tie bar arranged to connect the die pad and the side ring pad,

wherein said plurality of electrode pads includes power electrode pads which are electrically interconnected to the side ring pad by power bonding wires.

11. The semiconductor chip package as claimed in claim 10, wherein the die pad has a bottom surface exposed from the package body.

12. A semiconductor chip package comprising:

a semiconductor chip having an active surface where a plurality of

electrode pads are formed;

a lead frame having a plurality of leads;

a plurality of bonding wires electrically interconnecting the electrode pads and corresponding leads;

an encapsulant encapsulating the semiconductor chip, thereby forming a package body;

said lead frame comprising:

a die pad on which the semiconductor chip is mounted;

a plurality of inner leads electrically interconnected to corresponding electrode pads by a plurality of bonding wires;

a side ring pad disposed around the die pad and between the die pad and the inner leads;

a tie bar for connecting the die pad and the side ring pad; and

said side ring pad includes a plurality of metal pads formed thereon.

13. The semiconductor chip package as claimed in claim 12, wherein the plurality of bonding wires include first link bonding wires connected between the electrode pads and the metal pads and second link boding wires connected between the metal pads and the inner leads.

14. A lead frame comprising:

a die pad on which a semiconductor chip having a plurality of bond pads is mounted;

a side ring pad disposed around the die pad;

a power inner lead electrically connected to the side ring pad, the side ring pad being disposed between the die pad and the power inner lead; and

a tie bar arranged to connect the die pad and the side ring pad;

wherein said plurality of electrode pads include power electrode pads which are electrically interconnected to the side ring pad.

15. The lead frame of claim 14, wherein the power electrode pads are electrically interconnected to the side ring pad by power bonding wires.